Please cancel claim 44 without prejudice.

Please amend the claims as follows:

1-19.   (Cancelled)

20.   (Currently amended) A bus state keeper comprising:

a ~~plurality of multiplexers each having~~ plurality of units, each of the units comprising a multiplexer and a flip flop;

wherein each of the multiplexers includes:

a select input, the select input of being coupled with a respective select signal of a plurality of select signals;

an output, the output being coupled to a respective bit of a first bus, the first bus being coupled to a plurality of devices, wherein the first bus is to be kept in a steady state when inactive by the plurality of units,

a first input, the first input being coupled to a respective bit of a second bus, and

a second input, ~~and~~

wherein the second bus is selected as an input by the plurality of multiplexers,

~~an output,~~

the output coupled to each respective bit of a first bus coupled to a

plurality of devices, wherein the first bus is to be kept in a steady state when

inactive,

the first input coupled to each respective bit of a second bus,

wherein the select input of each of the plurality of multiplexers coupled to

a select signal;

and

a plurality of flip flops each having wherein each of the flip-flops includes:

a data input, the data input coupled to each respective bit of the first bus,

a data output, the data output coupled respectively to the second input of

the plurality of multiplexers, and

a clock input, the clock input coupled to a clock signal,

the data input coupled to each respective bit of the first bus,

the data output coupled respectively to the second input of the plurality of

multiplexers,

the clock input coupled to a clock signal, and

wherein the plurality of flip flops are to store a state of the first bus.

21.   (Previously presented) The bus state keeper of claim 20, wherein,

the plurality of flip flops are clocked by the clock signal to store a state of the first

bus.

22.   (Previously presented) The bus state keeper of claim 20, wherein,

the select signal input to each select input of the plurality of multiplexers selects

between

outputting a stored state in the flip flops onto the first bus

or

outputting the state of the second bus onto the first bus.

23.   (Previously presented) The bus state keeper of claim 20, wherein,

the select signal input to each select input of the plurality of multiplexers selects

to output from the plurality of multiplexers a stored state in the flip flops onto the first

bus to maintain a state of the first bus.

24.   (Previously presented) The bus state keeper of claim 23, wherein,

the select signal maintains a state of the first bus to conserve power.

25-39. (Cancelled)

40.   (Currently amended)   A bus state keeper for conserving power, the bus

state keeper comprising:

a plurality of flip flops to store a state of an output bus, the output bus having a

plurality of bits, each of the plurality of flip flops ~~having~~ including:

a data input, the data input of each flip flop being coupled to a respective

bit of the output bus,

a data output, and

a clock input, the clock input of each flip-flop being coupled to a clock

signal; and

~~wherein the data input of each flip flop is coupled to a respective bit of the~~

~~output bus, and~~

~~the clock input of each is coupled to a clock signal;~~

~~and,~~

a plurality of multiplexers coupled to the plurality of flip flops, an input bus, and

the output bus, each of the plurality of multiplexers ~~having~~ <u>including</u>:

a select input, <u>the select input of each multiplexer being coupled to a</u>

<u>respective select signal of a plurality of select signals,</u>

a first input, <u>the first input of each multiplexer being coupled to a</u>

<u>respective bit of the input bus,</u>

a second input, <u>the second input of each multiplexer is coupled to the data</u>

<u>output of a respective flip flop</u> and

an output, <u>the output of each multiplexer being coupled to a respective bit</u>

<u>of the output bus, wherein:</u>

<u>the input bus is selected by the plurality of multiplexers, and</u>

<u>the bus state keeper drives the state of the input bus onto the output</u>

<u>bus to change the state of the output bus.</u>

~~wherein the select input of each multiplexer is coupled to a select signal,~~

~~the first input of each multiplexer is coupled to a respective bit of the input~~

~~bus,~~

~~the second input of each multiplexer is coupled to the data output of a~~

~~respective flip flop, and~~

~~the output of each multiplexer is coupled to a respective bit of the output~~

~~bus.~~

41.   (Previously presented) The bus state keeper of claim 40, wherein,

the plurality of flip flops are clocked by the clock signal to store a state of the

output bus.

42.   (Currently amended) The bus state keeper of claim 40, wherein,

each of the plurality of flip flops [[are]] is a single bit D type flip flop.

43.   (Previously presented) The bus state keeper of claim 40, wherein , when

the output bus is selected to be output by the plurality of multiplexers, the bus state

keeper recycles the state of the output bus to keep it in a steady state and conserve power.

44.   (Cancelled)

45.   (Currently amended) A bus state keeper to couple between an input bus

and an output bus, the bus state keeper comprising:

a bus multiplexer to selectively couple a first bus input or a second bus input onto

a bus output in response to a select input, the bus multiplexer including a plurality of

single bit multiplexers, and wherein

the select input of the bus multiplexer is to couple to ~~a select signal~~ a

plurality of select signals,

the first bus input of the bus multiplexer is to couple to the input bus, and

the bus output of the bus multiplexer is to couple to the output bus;

and

a bus register to store a state of a data bus input and output the state at a data bus output in response to a clock input, the bus register including a plurality of single bit flip flops, and wherein

the data bus input of the bus register is to couple to the output bus,

the data bus output of the bus register is to couple to the second bus input of the bus multiplexer, and

the clock input to couple to a clock signal.

46. (Previously presented) The bus state keeper of claim 45, wherein,

the bus register is clocked by the clock signal to store a state of the output bus.

47. (Previously presented) The bus state keeper of claim 45, wherein,

the plurality of single bit flip flops of the bus register are D type flip flops.

48. (Previously presented) The bus state keeper of claim 45, wherein,

when the second bus input of the bus multiplexer is selected to be coupled onto the bus output by the bus multiplexer,

the bus state keeper to recycle the state of the output bus to keep it in a steady state and conserve power.

49. (Currently amended) The bus state keeper of claim 45, wherein [[,]] :

~~when the first bus input of the bus multiplexer is selected to be coupled onto the bus output by the bus multiplexer,~~

the bus state keeper to drive the state of the input bus onto the output bus to change the state of the output bus.

50.   (Currently amended) A bus state keeper for conserving power, the bus state keeper comprising:

a plurality of bit bus keepers coupled between bits of an input bus and bits of an output bus, the plurality of bit bus keepers to store a state of the bits of the output bus, each of the plurality of bit bus keepers including:

a flip flop to store a state of a respective bit of the output bus as a stored state, [[the]] each flip flop having:

a data input to couple to a respective bit of the output bus,

a data output,

a clock input to couple to a clock signal, and

a storage element coupled to the data input and the data output, the storage element to store the state of the data input in response to the clock input;

and,

a multiplexer coupled to the flip flop, the multiplexer to couple to a respective bit of the input bus and the respective bit of the output bus, the respective bit of the output bus coupled to a plurality of devices, the multiplexers to select an input bus for the bus state keeper, [[the]] each multiplexer having:

a select input to couple to a respective select signal of a plurality of select signals,

a first input to couple to the respective bit of the input bus,

a second input to couple to the data output of the flip flop, and

an output to couple to the respective bit of the output bus, and

wherein the multiplexer is adapted to selectively drive the

respective bit of the output bus with:

a state of the respective bit of the input bus to change the

state of the respective bit of the output bus

or

the stored state of the respective bit of the output bus to

maintain the state of the respective bit of the output bus.

51.   (Previously presented) The bus state keeper of claim 50, wherein,

the flip flop of each of the plurality of bit bus keepers is a D type flip flop.

52.   (Currently amended) The bus state keeper of claim 50, wherein,

the bus state keeper is to recycle the state of the bits of the output bus to keep it in

a steady state and conserve power in response to the select signal.

53.   (Previously presented) The bus state keeper of claim 20, wherein,

one of the plurality of devices coupled to the first bus is a flip flop of the plurality

of flip flops.

54.   (Previously presented) The bus state keeper of claim 53, wherein,

another one of the plurality of devices coupled to the first bus is a memory block.

55.   (Previously presented) The bus state keeper of claim 40, wherein,

one of the plurality of devices coupled to the output bus is a flip flop of the

plurality of flip flops.

56.   (Previously presented) The bus state keeper of claim 45, wherein,

one of the plurality of devices coupled to the output bus is a flip flop of the

plurality of flip flops.

57.   (Previously presented) The bus state keeper of claim 50, wherein,

one of the plurality of devices coupled to the respective bit of the output bus is the

flip flop.